## REMARKS

Claims 1-18 are currently pending, of which claims 1 and 14-18 are independent. Claims 1, 3-5, 13-15, 17, 18 have been amended. No new matter has been added. Reconsideration of the action mailed November 18, 2004, is requested in light of the forgoing amendments and the following remarks.

The Examiner provisionally rejected claims 1-6 and 17-18 under the doctrine of obviousness-type double patenting over claims 1-18 of co-pending U.S. Patent Application No. 10/024,303 to Lee et al. ("Lee").

The Examiner rejected claims 1-3, 5, 12, and 15-18 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,607,313 to Farries et al. ("Farries"). The Examiner rejected claims 4 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Farries in view of U.S. Patent No. 6,271,952 to Epworth ("Epworth"). The Examiner rejected claims 7-11 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Farries in view of U.S. Patent No. 4,768,848 to Vaerewyck ("Vaerewyck"). The Examiner rejected claim 13 under 35 U.S.C. § 103(a) as being unpatentable in view of Farries in view of U.S. Patent No. 5,111,322 to Bergano et al. ("Bergano"). Applicant traverses the rejections.

### Provisional Double Patenting Rejection

The Examiner has provisionally rejected claims 1-6 and 17-18 under the doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of Lee. Applicant respectfully traverses the rejection. Independent claims 1, 13, and 18 of Lee are patently distinct from claims 1-6 and 17-18 because, at least, claims 1, 13, and 18 of Lee recite features not set forth in claims 1-6 or 17-18 of the present application. Claims 1-18 of Lee recite an optical delay switching and combining array not found in claims 1-6 and 17-18 of the present application. Additionally, claims 1-6 and 17-18 of the present application recite an integrated modulator chip for generating optical Return-to-Zero signal streams, which is not found in claims 1-18 of Lee.

**Section 102(e) Rejections**

Claim 1 stands rejected as anticipated by Farries. Claim 1, as amended, is directed towards an integrated optical time division multiplexing module that includes an integrated time-delay chip having a plurality of waveguides operable to guide the at least first and second optical Return-to-Zero signal streams through the integrated time-delay chip.

The Examiner states that Farries discloses Applicant's claimed integrated time-delay chip as a combination of a glass spacer 17, silicon spacer 18, and birefringent crystal 14 of FIGS. 7 and 8. Applicant respectfully disagrees. Farries discloses a time-division multiplexing device. The device includes a wavelength chip that includes a pair of modulators for modulating an input laser signal into first and second modulated signals. *See* col. 5, lines 48-62. The wavelength chip is optically coupled to a delay and interleaving structure that includes a half waveplate and a birefringent crystal. *See* col. 5, lines 41-47. The polarization of the second modulated signal is rotated before entering the birefringent crystal such that the first and second modulated signals are orthogonally polarized. *See* col. 6, lines 15-18. The orthogonal polarization of the second modulated signal causes the signal to bend within the birefringent crystal towards the first modulated signal such that the first and second modulated signals join in the birefringent crystal. *See* col. 6, lines 44-56. The longer path of the second modulated signal traveling to rejoin the first modulated signal, within the birefringent crystal, produces a desired time delay. *See* col. 6, lines 17-27.

Farries fails to disclose or suggest an integrated time-delay chip. Instead, Farries discloses a combination of separate optical components that delay and combine light signals when optically coupled to the modulator chip. A combination of coupled optical components does not disclose or suggest a chip. Additionally, Farries fails to disclose or suggest a time-delay chip having a plurality of waveguides operable to guide optical Return-to-Zero signals through the time-delay chip. There are no waveguides in Farries' waveplate and birefringent crystal combination. Therefore, there are no waveguides in Farries' time-delay apparatus. Applicant respectfully submits that claim 1, as well as claims
2-13, which depend from claim 1, are in condition for allowance.

Claim 5 stands rejected as anticipated by Farries. Claim 5 is directed towards an integrated optical time division multiplexing module that includes a time-delay chip including first and second waveguides where one of the first and second waveguides is of greater length than the other waveguide. As discussed above, Farries does not disclose or suggest a time-delay chip that includes any waveguides. Therefore, Farries also fails to disclose or suggest a time-delay chip that includes waveguides of different lengths. Applicant respectfully submits that claim 5, as well as claim 6, which depends from claim 5, is in condition for allowance.

The Examiner states that Farries discloses the claimed first and second waveguides at FIGS. 4, 7, and 8 and col. 6, lines 30-60. The cited sections of Farries only disclose the time-delay apparatus described above that includes a combination of a glass spacer, silicon spacer, and birefringent crystal. Farries does not disclose or suggest a time-delay chip that includes waveguides. For at least the same reasons set forth above with respect to claim 1, claim 5 as well as claim 6, which depend from claim 1, are in condition for allowance.

Claim 15 stands rejected as anticipated by Farries. Claim 15 is directed towards an integrated optical time division multiplexing module that includes an integrated time-delay chip having first and second waveguides operable to guide the first and second optical Return-to-Zero signal streams through the integrated time-delay chip. For at least the same reasons set forth above with respect to claim 1, claim 15 is in condition for allowance.

Claim 16 stands rejected as anticipated by Farries. Claim 16 is directed towards an integrated optical time division multiplexing module that includes an integrated time-delay chip having first and second waveguides, each waveguide carrying an optical signal stream. For at least the same reasons set forth above with respect to claim 1, claim 16 is in condition for allowance.

Claim 17 stands rejected as anticipated by Farries. Claim 17 is directed towards an integrated optical time division multiplexing module that includes first and second waveguides adapted to divide an incoming signal stream into first and second signal streams for transmission along the first and second waveguides. For at least the same reasons set forth above with respect to claim 1, claim 17 is in condition for allowance.

Additionally, claim 17 includes an integrated modulator chip having an end facet that is coated with a reflective coating to reflect a first and second optical Return-to-Zero signal streams along first and second waveguides of the integrated modulator chip towards the first and second waveguides of the integrated time-delay chip. Farries does not disclose or suggest any reflective coating for reflecting optical signals along a first and second waveguide. For at least this additional reason, claim 17 is allowable.

Claim 18 stands rejected as anticipated by Farries. Claim 18 is directed towards an integrated optical time division multiplexing module that includes an integrated time-delay chip that includes a plurality of waveguides operable to guide the plurality of optical Return-to-Zero signal streams through the integrated time-delay chip. For at least the same reasons set forth above with respect to claim 1, claim 18 is in condition for allowance.

**Section 103(a) Rejections**

Claim 14 stands rejected as unpatentable over Farries in view of Vaerewyck. Claim 14 is directed towards an integrated optical time division multiplexing module that includes an integrated time-delay chip including first and second waveguides operable to guide the first and second optical Return-to-Zero signal streams through the integrated time-delay chip.

The Examiner states that Farries discloses Applicant's claimed integrated time-delay chip as glass spacer 17, silicon spacer 18, and birefringent crystal 14 of FIGS. 7 and 8. As discussed above with respect to claim 1, Farries does not disclose an integrated time-delay chip that includes waveguides. For at least the same reasons as set forth with respect to claim 1, Farries does not disclose or suggest a time-delay chip including first and second waveguides.

Vaerewyck discloses an optical repeater. *See* Abstract; col. 3, lines 33-35. Vaerewyck does not disclose or suggest an integrated time-delay chip including first and second waveguides. Applicant respectfully submits that claim 14 is in condition for allowance.

Applicant respectfully requests that all pending claims be allowed. Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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